

CLAIMS

We claim:

1. A semiconductor memory device, comprising:
a first chip adapted to generate a first ready/busy signal, the first ready/busy signal indicating the first chip is busy; and
a second chip adapted to generate a second ready/busy signal, the second ready/busy signal indicating the second chip is busy;
where the first ready/busy signal is distinct from the second ready/busy signal.

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2. The semiconductor memory device of claim 1
where the first chip is adapted to operate responsive to a first chip enable signal; and
where the second chip is adapted to operate responsive to a second chip enable signal.
3. The semiconductor memory device of claim 1
where the first and second chips are adapted to operate responsive to control signals from a host.
4. The semiconductor memory device of claim 1 comprising:
a third chip connected in parallel with the first chip; and
a fourth chip connected in parallel with the second chip;
where the first ready/busy signal indicates the third chip is busy; and
where the second ready/busy signal indicates the fourth chip is busy.
5. The semiconductor memory device of claim 4
where the third chip is adapted to operate responsive to a first chip enable signal; and
where the fourth chip is adapted to operate responsive to a second chip enable signal.
6. A device, comprising:
first chip means for generating a first status signal; and
second chip means for generating a second status signal, the second status signal being distinct from the first status signal.

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7. The device of claim 6

where the first chip means operates responsive to a first enable signal; and
where the second chip means operates responsive to a second enable signal.

8. The device of claim 7

where the first and second chip means operate responsive to control signals.

9. The device of claim 8 comprising:

third chip means for generating the first status signal; and

10 fourth chip means for generating the second status signal;

where the first status signal indicates the first or third chip means are busy; and

where the second status signal indicates the second or fourth chip means are busy.

10. The device of claim 9

where the third chip means is adapted to operate responsive to the first chip enable signal; and

where the fourth chip means is adapted to operate responsive to the second chip enable signal.